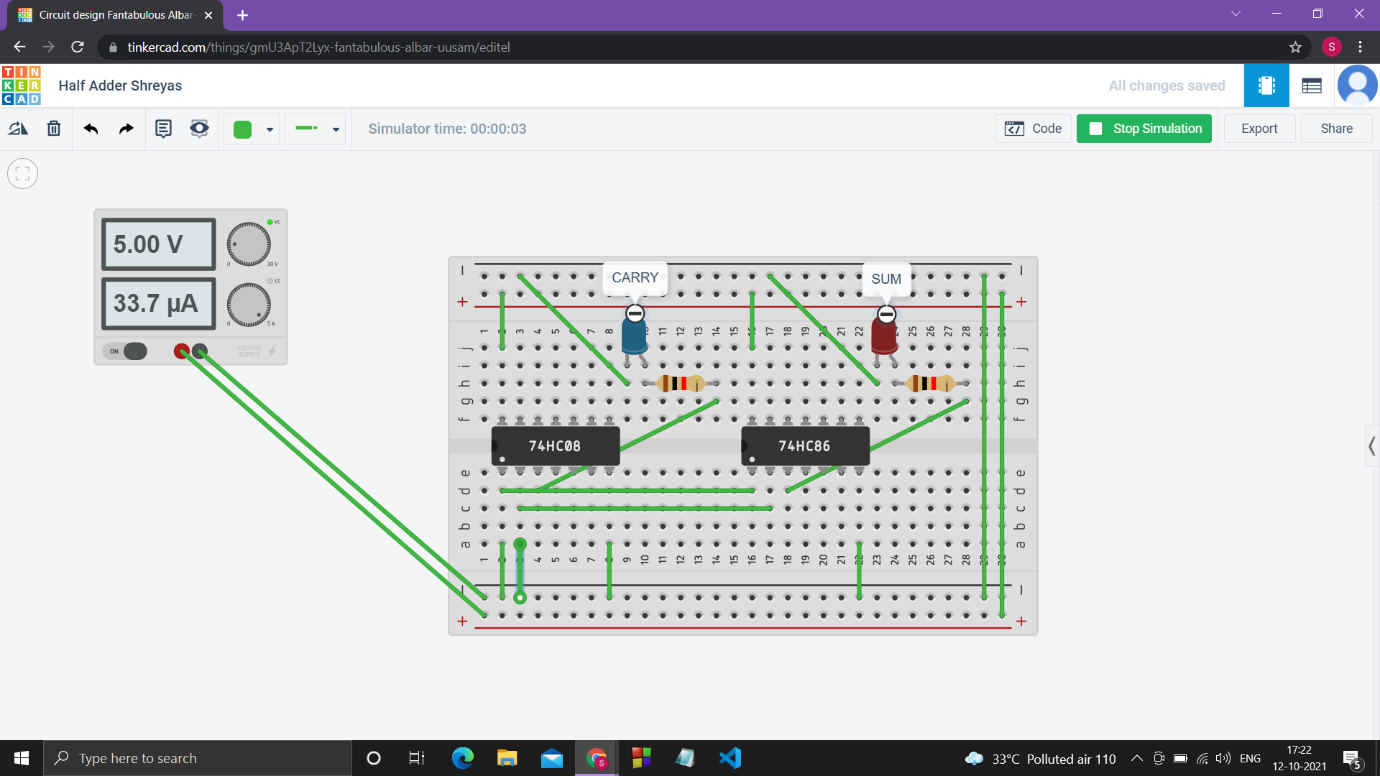
LAB 2: IMPLEMENTING HALF AND FULL ADDER USING LOGIC GATES

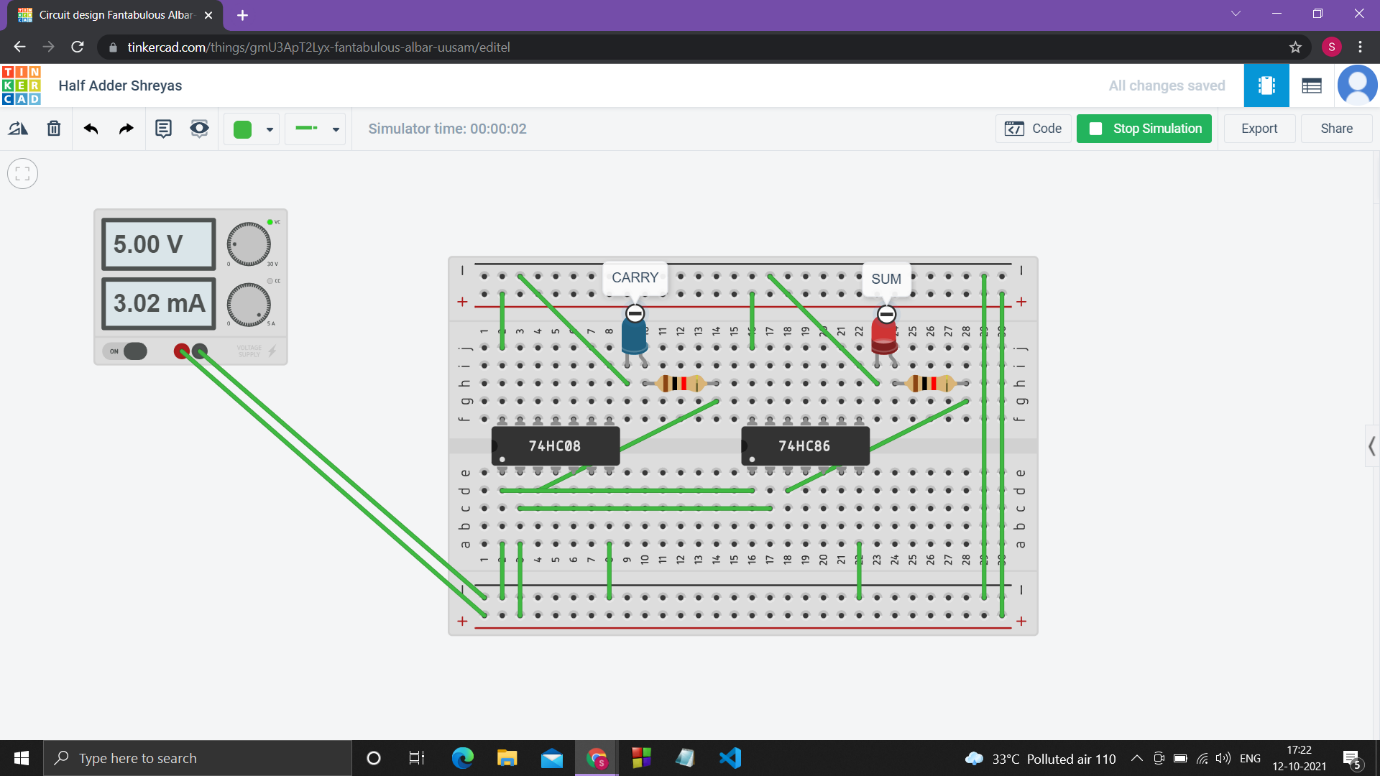
Name: Shreyas Sawant Div: D7A Roll No.: 55

1) Half Adder

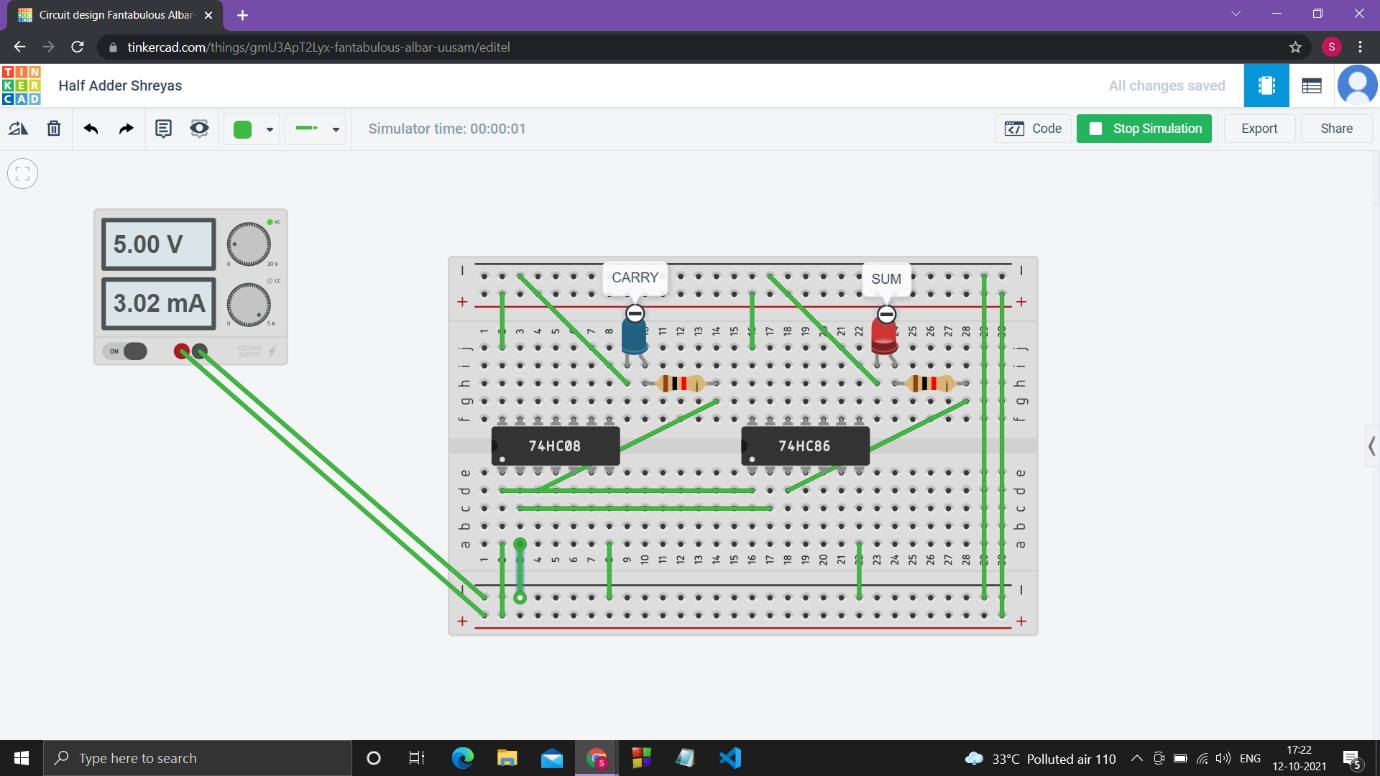
A=0 B=0



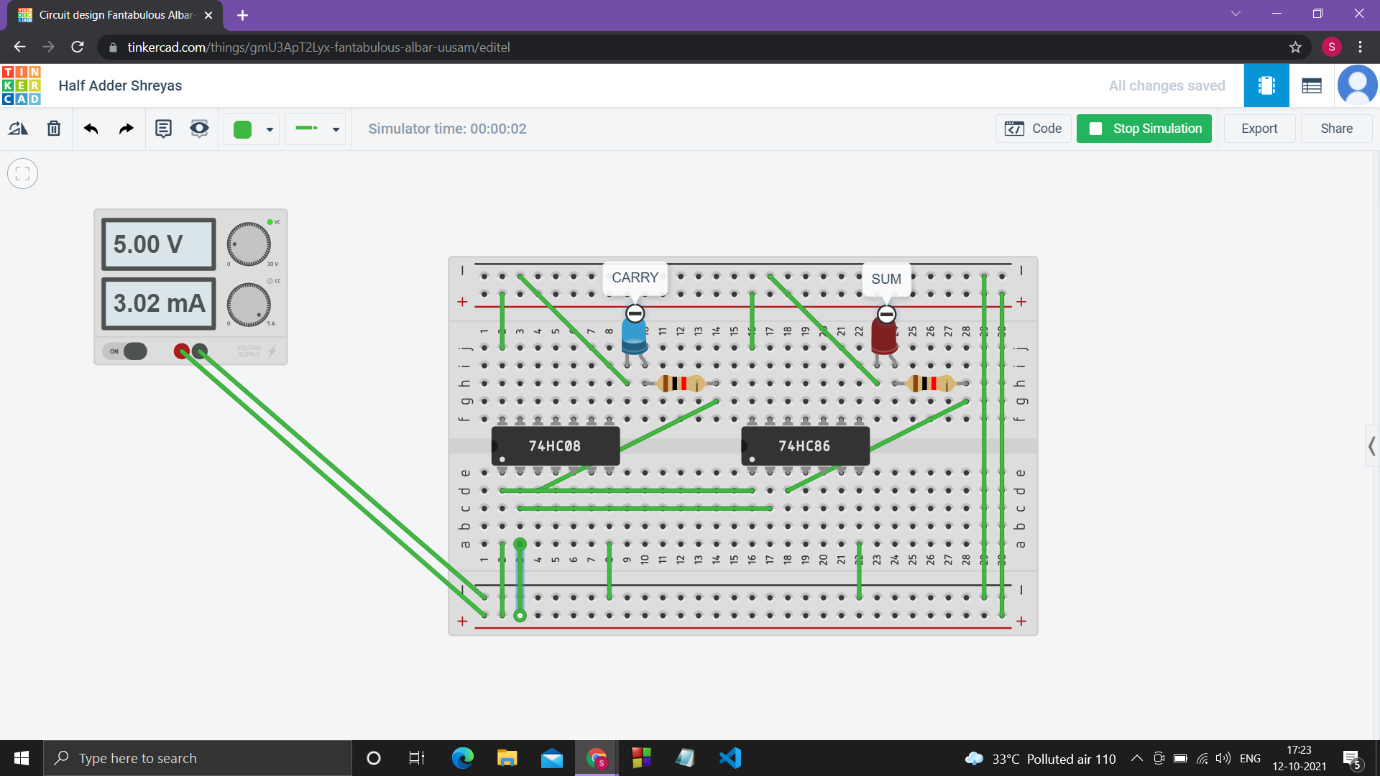
A=0 B=1



A=0 B=1

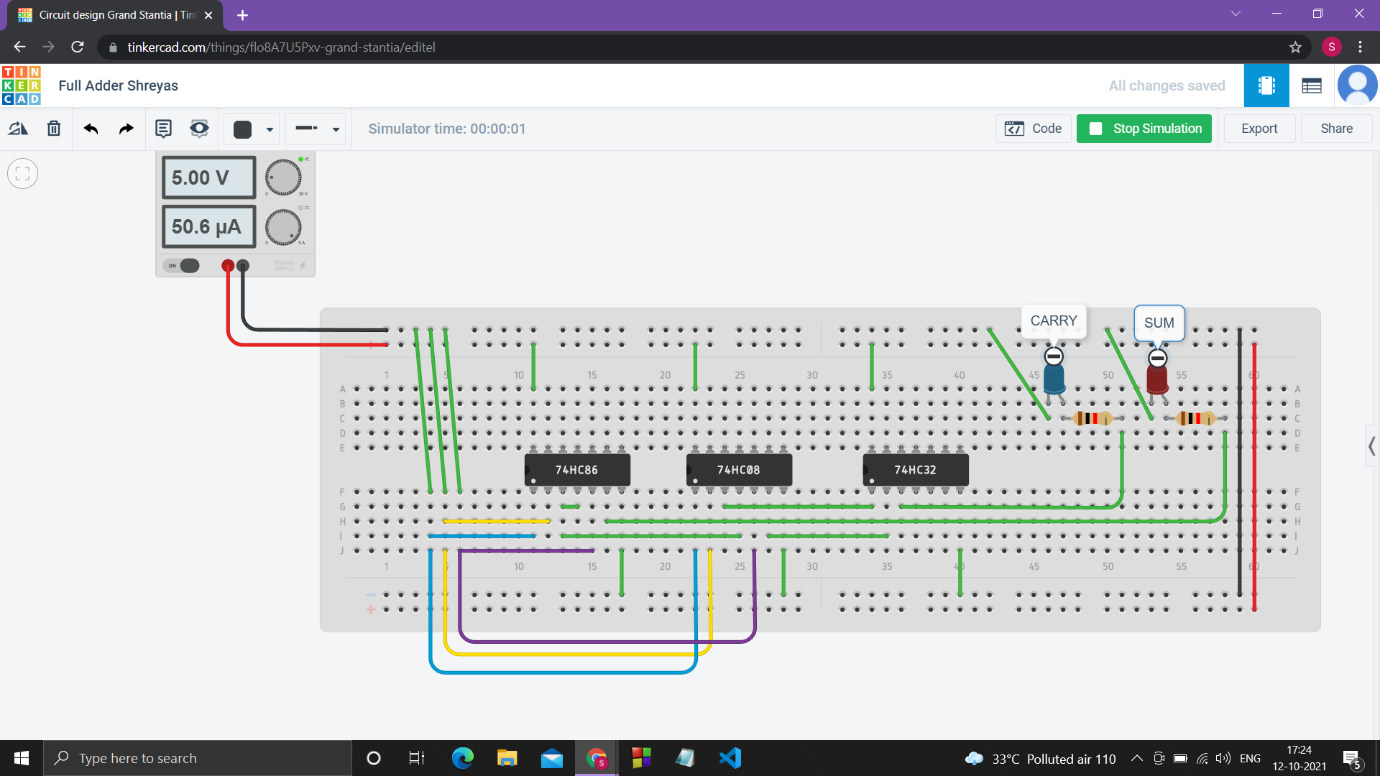


A=1 B=1

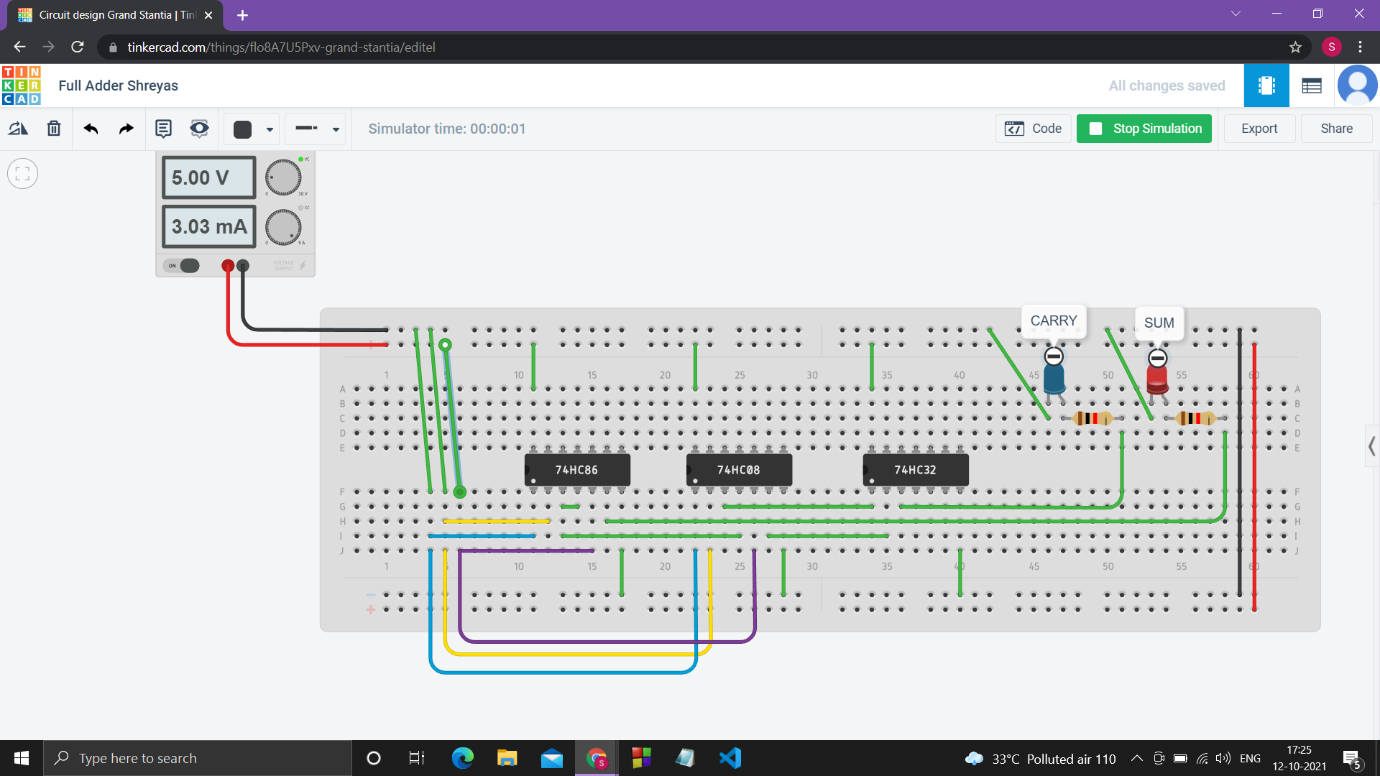


2) Full Adder

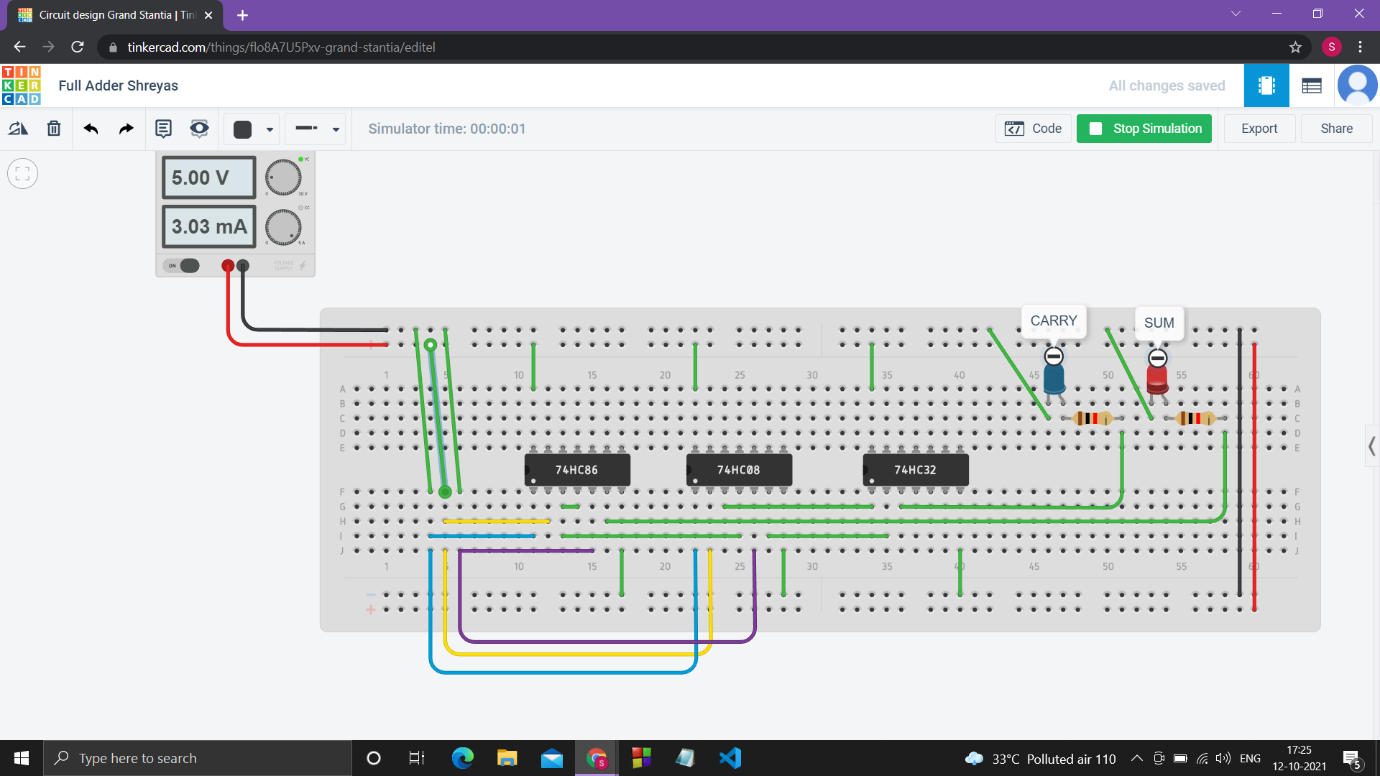
A=0 B=0 C=0



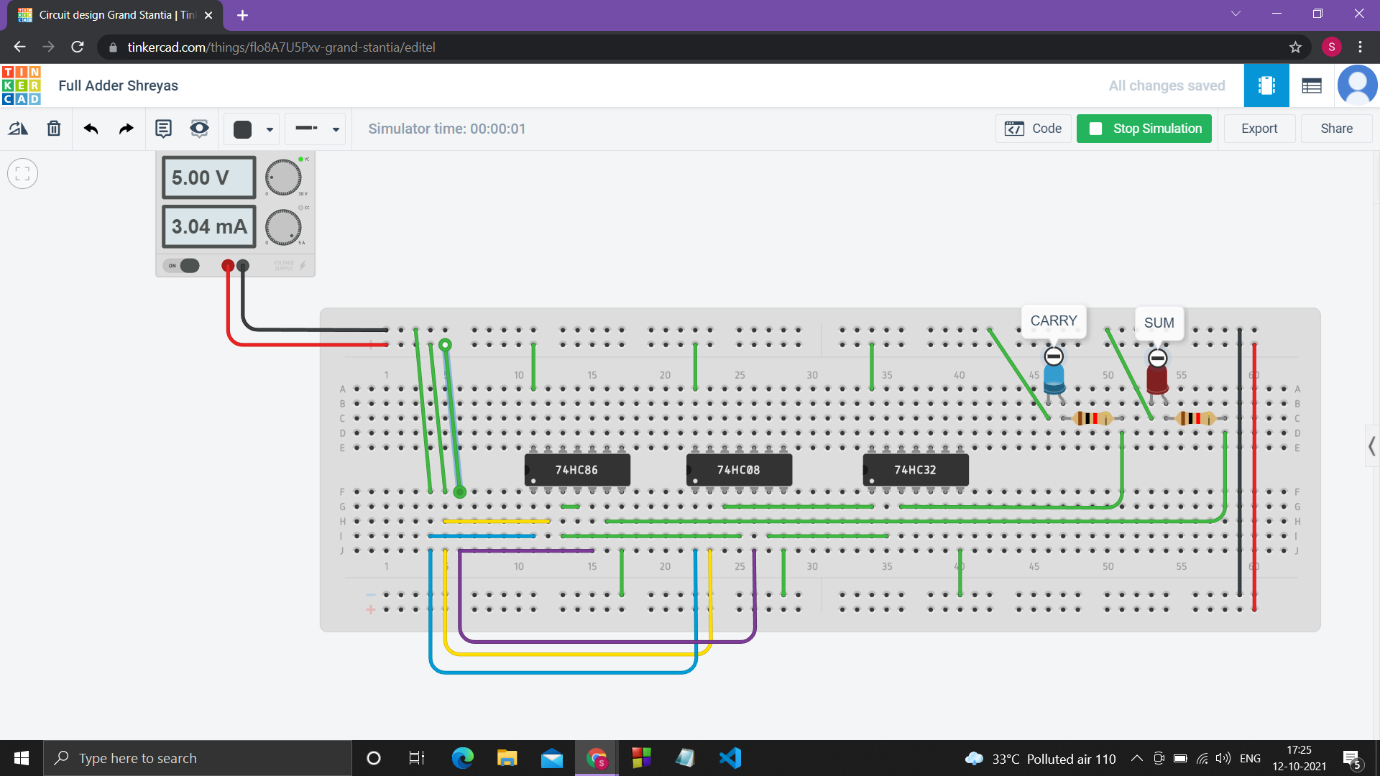
A=0 B=0 C=1



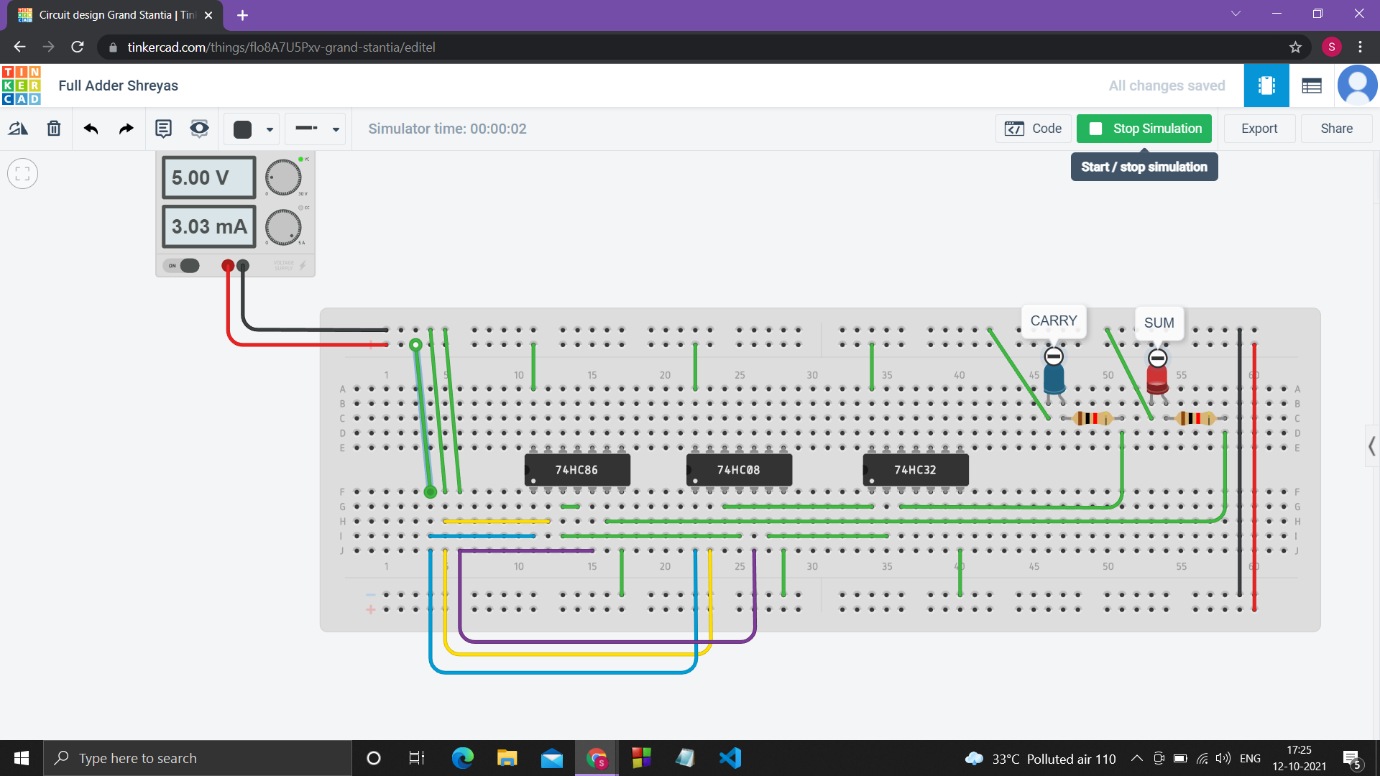
A=0 B=1 C=0



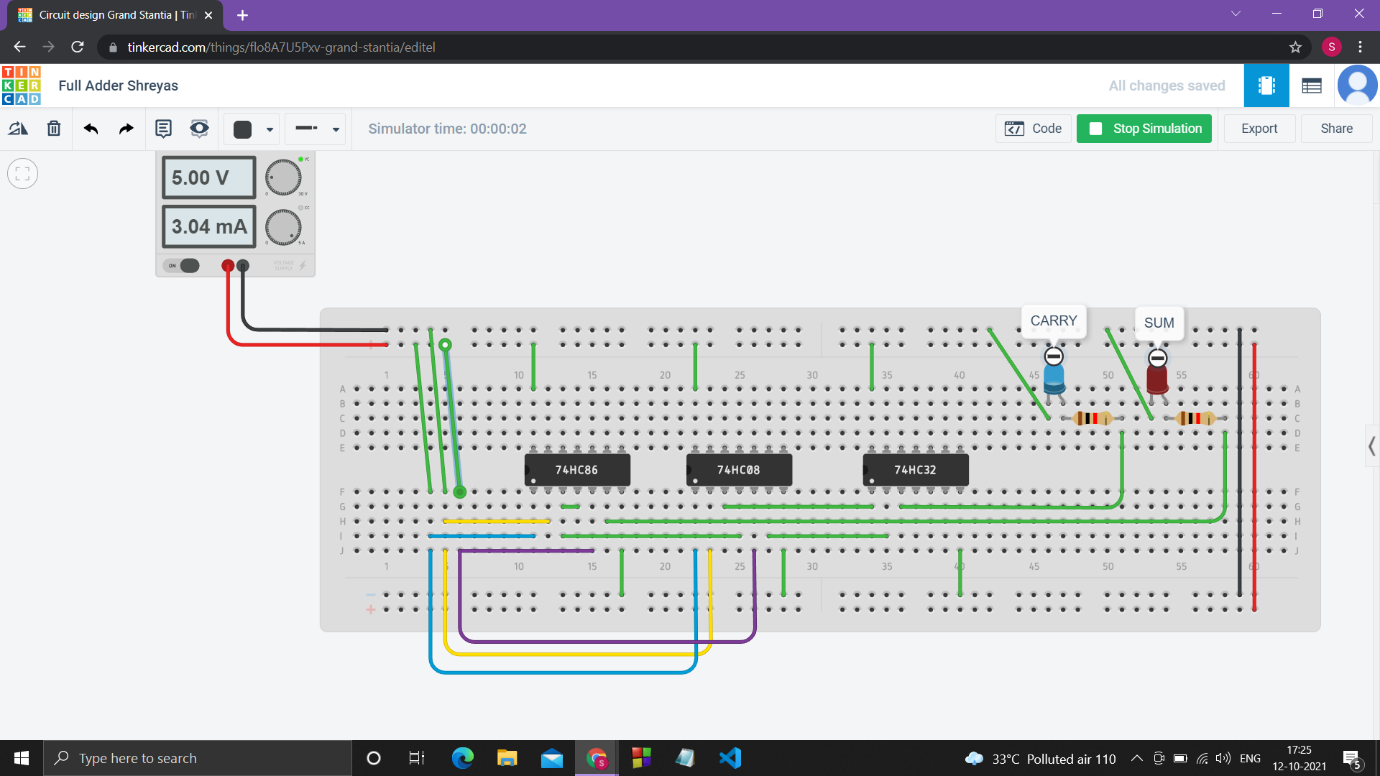
A=0 B=1 C=1



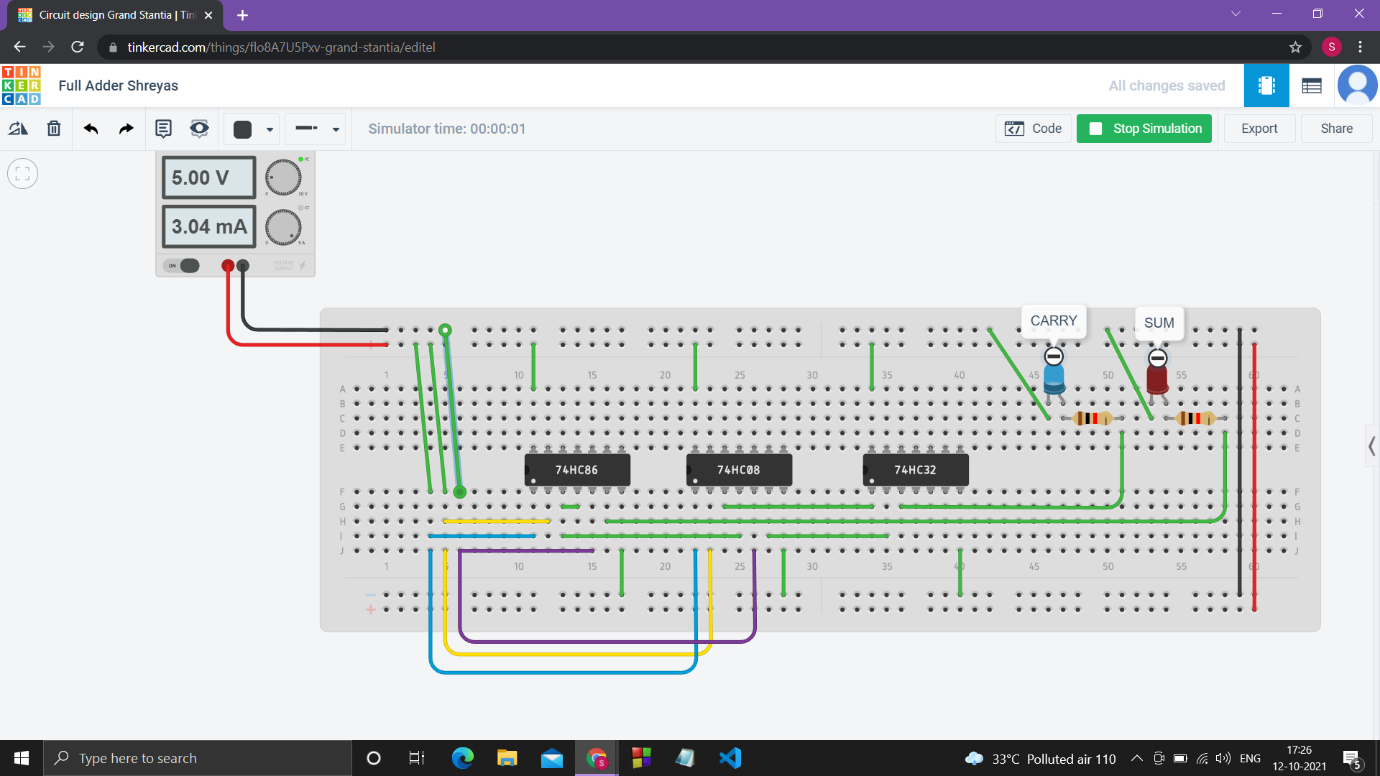
A=1 B=0 C=0



A=1 B=0 C=1



A=1 B=1 C=0



A=1 B=1 C=1

